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1 System-level power optimization: techniques and tools
Luca Benini, Giovanni de Micheli
April 2000   **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2
Publisher: ACM Press
Full text available: 📄 pdf(385.22 KB)   Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems con
platform and software layers. We consider the three major constituents of hardware that consume energy, name
communication, and storage units, and we review methods of reducing their energy consumption. We also study
energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

2 Special issue: AI in engineering
D. Sriram, R. Joobbani
April 1985   **ACM SIGART Bulletin**, Issue 92
Publisher: ACM Press
Full text available: 📄 pdf(8.79 MB)   Additional Information: full citation, abstract

The papers in this special issue were compiled from responses to the announcement in the July 1984 issue of the
notices posted over the ARPAnet. The interest being shown in this area is reflected in the sixty papers received fr
About half the papers were received over the computer network.

3 GPGPU: general purpose computation on graphics hardware
David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn
August 2004   **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**
Publisher: ACM Press
Full text available: 📄 pdf(63.03 MB)   Additional Information: full citation, abstract, citings

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flex
graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully progran
processing units that support vector operations up to full IEEE floating point precision. High level languages have
hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

4 Formal verification in hardware design: a survey
Christoph Kern, Mark R. Greenstreet
April 1999   **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2
Publisher: ACM Press

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181 Proceedings of the SIGNUM conference on the programming environment for development of numerical s
March 1979   **ACM SIGNUM Newsletter**, Volume 14 Issue 1
Publisher: ACM Press
Full text available: 🔲 pdf(5.02 MB)   Additional Information: full citation

182 Model-based recognition in robot vision
Roland T. Chin, Charles R. Dyer
March 1986   **ACM Computing Surveys (CSUR)**, Volume 18 Issue 1
Publisher: ACM Press
Full text available: 🔲 pdf(4.94 MB)   Additional Information: full citation, abstract, references, citings, index terms, revi

> This paper presents a comparative study and survey of model-based object-recognition algorithms for robot visic
> algorithms is to recognize the identity, position, and orientation of randomly oriented industrial parts. In one forr
> referred to as the "bin-picking" problem, in which the parts to be recognized are presented in a jumbled bin. The
> according to 2-D, 2½-D, and 3-D object representations, which are used as the basis for ...

183 Power minimization in IC design: principles and applications
Massoud Pedram
January 1996   **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1
Publisher: ACM Press
Full text available: 🔲 pdf(550.02 KB)   Additional Information: full citation, abstract, references, citings, index terms

> Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused
> in which power dissipation is as important as performance and area. This article presents an in-depth survey of C
> techniques for designing low power digital CMOS circuits and systems and describes the many issues facing desi
> logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

> **Keywords**: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy
> clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, powe
> minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switch
> switching activity, symbolic simulation, synthesis, system design

184
Process migration

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	6702	(debug$3 or test$3 or check$3 or verif$3) same electronic same design	US-PGPUB; USPAT	OR	ON	2006/11/24 22:15
L2	55950	signal same (output$3 or "i/o" or "i/os") near3 (pin or pad or port) same (path or line or route or routing or interconnect$4 or connect$4 or wire or wiring)	US-PGPUB; USPAT	OR	ON	2006/11/24 22:15
L3	5798	quantity near4 register	US-PGPUB; USPAT	OR	ON	2006/11/24 22:16
L4	44167	(compil$5 or recompil$5 or synthes$4) near5 (incremental$3 or partial$3 or part or portion)	US-PGPUB; USPAT	OR	ON	2006/11/24 22:17
L5	11035	synchroniz$3 same internal same signal	US-PGPUB; USPAT	OR	ON	2006/11/24 22:18
L6	383	(path or line or route or routing or interconnect$4 or connect$4 or wire or wiring) adj (netlist or "net list")	US-PGPUB; USPAT	OR	ON	2006/11/24 22:18
L7	1570	(716/1).ccls.	US-PGPUB; USPAT	OR	ON	2006/11/24 22:18
L8	503	(714/39).ccls.	US-PGPUB; USPAT	OR	ON	2006/11/24 22:19
L9	248	(714/725).ccls.	US-PGPUB; USPAT	OR	ON	2006/11/24 22:19
L10	934	(714/733).ccls.	US-PGPUB; USPAT	OR	ON	2006/11/24 22:22
L11	1785	(714/724).ccls.	US-PGPUB; USPAT	OR	ON	2006/11/24 22:19
L12	505	(714/37).ccls.	US-PGPUB; USPAT	OR	ON	2006/11/24 22:20
L13	16	1 and 2 and 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/24 22:20
L14	7	13 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/24 22:20

L15	0	14 and 5 and 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/24 22:21
L16	0	14 and 5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/24 22:21
L17	19	1 and 3 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/24 22:21
L18	1	17 and (7 or 8 or 9 or 10 or 11 or 12)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/24 22:22
L19	6	17 and ("714"/$).ccls.	US-PGPUB; USPAT	OR	ON	2006/11/24 22:22